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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SOLOMON, GARY L	

ART UNIT	PAPER NUMBER
2615	8

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/620,498	HAGIHARA, YOSHIO	
	Examiner	Art Unit	
	Gary L Solomon	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/20/04* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-8,10-18,20,23 and 24* is/are pending in the application.

4a) Of the above claim(s) *4,5,9,19,21 and 22* is/are withdrawn from consideration.

5)☒ Claim(s) *8,17,20,23 and 24* is/are allowed.

6)☒ Claim(s) *1-3 and 6-8, 11,14, and 16* is/are rejected.

7)☒ Claim(s) *10,12,13 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Species 7 in Paper No. 7 is acknowledged.

2. Claims 4-5, 9, 19, 21, and 22 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 7.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-3, 11, and 16 are rejected under 35 U.S.C. 102(a) as being anticipated by Moose (Self Calibrating Logarithmic CMOS Image Sensor).

For claim 1, Moose discloses an image-sensing apparatus (abstract) comprising: a plurality of pixels (section 2.2: Sensor Architecture); a photoelectric conversion portion (fig. 1) that has a photosensitive element (fig. 1, Photodiode) for producing an electric signal in accordance with amount of incident light and that outputs a signal obtained by converting the electric signal natural logarithmically (Abstract); and a lead-out path by way of which the signal output from the photoelectric conversion portion is fed to an output signal line (fig. 1: Vout); and a controller that detects a variation in sensitivity of the photoelectric conversion portion of each pixel by injecting an electric charge into the

photoelectric conversion portion (Abstract; section 2: Sensor Concept and Implementation).

For claim 2, Moose discloses all the previous limitations, and also wherein the pixels are arranged a matrix (fig. 2: pixel array).

For claim 3, Moose discloses all the previous limitations wherein the pixels each further comprise an integrator circuit that integrates the signal output from the photoelectric conversion portion so that a signal integrated by the integrator circuit is fed by way of the lead-out path to the output signal line (section 1: Introduction, 2nd paragraph).

For claim 11, Moose discloses all the previous limitations, wherein the lead-out path includes a switch that selects one after another of the pixels in a predetermined sequence and feeds the signal output from the selected pixel to the output signal line (section 2.1:Photoreceptor Circuit, also fig. 1).

For claim 16, Moose discloses all the previous limitations; the controller detects variations in sensitivity of the photoelectric conversion portion of the individual pixels with the photosensitive elements of the individual pixels kept in a dark state (section 3.1: Photorecepture Response, and fig. 4).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moose (Self Calibrating Logarithmic CMOS Image Sensor) in view of Kuroda (6,512,543).

For claim 6, Moose discloses all the previous limitations, but lacks the limitations set forth in claims 6-8. In claim 6, Moose discloses the CMOS imaging apparatus as recited in claim 6, but lacks teaching wherein the pixels each further comprise an amplifying transistor that amplifies the signal output from the photoelectric conversion potion so that a signal output is fed by way of the lead of the lead-out path to the output signal line.

Still, Moose does disclose a CMOS image sensor and photoelectric conversion portion that has an output signal line. In Kuroda, it is well known to amplify signals with a transistor from the photoelectric conversion on the output signal line in order to raise their signal strength and intensity (col. 2, lines 29-30, col. 6, lines 20-22).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to add an amplifying transistor to the CMOS imaging sensor of Moose in order to raise its signal strength and intensity as taught in Kuroda.

For claim 7, it is known in the art to use a CMOS imaging sensor for the previous limitations. However, Moose does not teach the requirements and limitations as further comprising: load resistors or constant current sources connected to the output signal line, a total number of the load resistors or constant current sources being smaller than a total number of pixels.

Nevertheless, Kuroda teaches a CMOS image sensor wherein constant current sources (Figure 1, Element 44) are connected to the output signal line (Figure 1, Element

43), a total number of constant sources being smaller than the total number of pixels (There are 3 constant current sources for 9 pixels).

The combination of the constant current sources would have been obvious; both the inventions of Moose and Kuroda are of CMOS image sensors. The load transistor in Kuroda serves as a constant current source for the source follower circuit including the load transistor and it determines an electric current flowing in that source follower circuit (Column 7, Line 60 through Column 8, line 9).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to configure the invention of CMOS image sensor of Moose with the constant current source of Kuroda in order to determine the current flowing through the source follower circuit.

For claim 8, Kuroda further discloses wherein the constant-current sources each comprise a resistive transistor (Figure 1, Element 44) having a first electrode connected to the output signal line (Figure 1, Element 44), a second electrode connected to a direct-current voltage, and a control electrode connected to a direct-current voltage (Figure 1, Element 44).

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moose (Self Calibrating Logarithmic CMOS Image Sensor) in view of Hynecek (US 6,323,479).

For claims 14, Moose discloses all the previous limitations, yet lacks teaching wherein, during image sensing, the pixels can operate selectively either in a first state in which the photoelectric conversion portion converts the electric signal linearly and in a second state in which the photoelectric conversion portion converts the electric signal natural logarithmically.

However, Hynecek teaches a sensor pixel linear and logarithmic response, further disclosing, during image sensing, the pixels can operate selectively either in a first state in which the photoelectric conversion portion converts the electric signal linearly and in a second state in which the photoelectric conversion portion converts the electric signal natural logarithmically (Abstract, Column 2, Line 60 through Column 3, Line 31). The logarithmic range begins after the region of sub-threshold conduction begins. The device of Hynecek provides for two regions of predetermined voltage. When the first predetermined is exceeded, the logarithmic response begins. When the second predetermined voltage is reached, the linear response begins.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to configure solid state imaging device of Moose with the sensor pixel with linear and logarithmic response of Hynecek in order to provide a pixel with an increased output signal swing into logarithmic response region (Column 2, Lines 12-13).

Allowable Subject Matter

8. Claims 17, 18, 20, 23, and 24 allowed.

9. The following is a statement of reasons for the indication of allowable subject matter:..

The closest prior art found in the examiners search does not include all the limitations listed in Claim 17. Those limitations include the following:

a second MOS transistor having a first electrode connected to the gate electrode of the first MOS transistor, a second electrode to which a direct-current voltage is applied, and a gate electrode;

a third MOS transistor having a first electrode connected to the gate electrode of the first MOS transistor, a second electrode connected to the first electrode of the first MOS transistor, and a gate electrode; and

a fourth MOS transistor having a first electrode, a second electrode,

and a gate electrode connected to the first electrode of the first MOS transistor; and a controller that detects variations in sensitivity of the individual pixels by feeding a signal to the gate electrode of the second MOS transistor so as to turn on the second MOS transistor and turning off the third MOS transistor so that a predetermined direct-current voltage is applied to the gate electrode of the first MOS transistor and that the gate electrodes of the first and fourth MOS transistors are brought into a cut-off state,

wherein the controller makes the individual pixels perform image sensing by turning off the second MOS transistor and feeding a signal to the gate electrode of the third MOS transistor so as to turn on the third MOS transistor so that the gate electrodes of the first and fourth MOS transistors are brought into a connected state.

10. Claims 18, 20, 23, and 24 are dependent upon Claim 17.

11. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not disclose the following limitations as recited in claim 12. The limitations include:

the photosensitive element having a first electrode to which a direct current voltage is applied and a second electrode; a first transistor having a first electrode connected to the

second electrode of the photosensitive element, a second electrode, and a control electrode,

the first transistor receiving an output current from the photoelectric element; and

a second transistor having a first electrode to which a direct-current voltage is applied, a second electrode from which an electric signal is output, and a control electrode connected to the first electrode of the first transistor, and wherein the pixels each further comprise:

a first switching portion for applying a direct-current voltage to the control electrode of the first transistor; and a second switching portion provided between the control electrode of the first transistor and the control electrode of the second transistor,

wherein the controller detects variations in sensitivity of the individual pixels by turning on the first switching portion and turning off the second switching portion so that a predetermined direct-current voltage is applied to the control electrode of the first transistor and that the control electrodes of the first and second transistors are brought into a cut-off state, and

wherein the controller makes the individual pixels perform image sensing by turning off the first switching portion and turning on the second switching portion so that the control electrodes of the first and second transistors are brought into a connected state.

13. Claims 13 and 15 are dependent upon Claim 12.

14. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matter: The prior art fails to disclose the following limitation:

wherein a direct current voltage applied to a first electrode of the amplifying transistor is lower that a direct current voltage applied to the second electrode of the resistive transistor.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L Solomon whose telephone number is (703)-305-4370. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vu Le can be reached on (703)-308-6613.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Or faxed to:

(703) 872-9314, (for informal or draft communications, please label "Proposed" or "Draft")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application should be directed to the customer service number **(703) 306-0377**.

March 8, 2004

VU LE
PRIMARY EXAMINER